WHAT IS CLAIMED IS:

1. A computational unit in an adaptable computing engine, wherein the computational unit includes a clock signal for determining a processor cycle, the computational unit comprising

one or more functional units coupled by a bus, wherein the one or more functional units include functional unit inputs;

at least one register coupled between the bus and at the input of least one functional unit input; and

a control signal for selectively causing the at least one register to hold a data value from the bus for one or more processor cycles.

2. The computational unit of claim 1, wherein the register includes circuitry for selectively providing a constant value.

3. The computational unit of claim 1, further comprising

a coupling of a pair of registers such that the pair of registers is responsive to a control signal value.

4. The computational unit of claim 3, further comprising

control circuitry for setting the pair of registers into predetermined states based on the control signal value.

5. The computational unit of claim 4, wherein the pair of registers includes first and second registers, wherein the predetermined states include one or more of the following for the first and second registers, respectively: load, hold; load, clear; hold, load; clear, load; hold, hold; hold, clear; clear, hold; and clear, clear.

6. The computational unit of claim 4, wherein the control signal value comprises 7 bits.

7. A method for providing data in a computational unit in an adaptable computing engine, the method comprising

including registers at inputs to functional units, wherein the registers are coupled to a bus for obtaining data from the bus;

including a control signal for selectively causing the registers to hold a data value from the bus for one or more processor cycles.

8. The method of claim 7, wherein the register includes circuitry for selectively providing a constant value.

9. The method of claim 7, further comprising coupling a pair of registers such that the pair of registers is responsive to a control signal value.

10. The method of claim 9, further comprising providing control circuitry for setting the pair of registers into predetermined states based on the control signal value.

11. The computational unit of claim 9, wherein the pair of registers includes first and second registers and wherein the predetermined states include one or more of the following for the first and second registers, respectively: load, hold; load, clear; hold, load; clear, load; hold, hold; hold, clear; clear, hold; and clear, clear.

12. The computational unit of claim 9, wherein the control signal value comprises 7 bits.

13. An apparatus for providing a data value in a computational unit in an adaptable computing engine, wherein the computational unit includes a multi-stage execution pipeline, the apparatus comprising

one or more functional units coupled by a bus, wherein the one or more functional units include functional unit inputs;

at least one input register coupled between the bus and at least one functional unit input; and

a data path from an input register to a given stage in the execution pipeline so that a value provided by the register is available for use at a time of execution of the given stage.

14. The apparatus of claim 13, wherein the register includes circuitry for selectively providing a constant value.

15. A method for providing a data value in a computational unit in an adaptable computing engine, wherein the computational unit includes a multi-stage pipeline, the method comprising

coupling one or more functional units to a bus, wherein the one or more functional units include functional unit inputs;

coupling at least one register between the bus and at least one functional unit input; and

providing a data path from a register to a given stage in the execution pipeline so that a value provided by the register is available for use at a time of execution of the given stage.

16. The apparatus of claim 13, wherein the register includes circuitry for selectively providing a constant value.